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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,553	07/10/2001	Fritz Gfeller	CH920000038US1/954-010307	7180

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EXAMINER	
FLANAGAN, KRISTA M	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/902,553	GFELLER ET AL.	
	Examiner	Art Unit	
	Krista M. Flanagan	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16 and 25* is/are allowed.

6)☒ Claim(s) *1,5-12,17,20-22 and 24* is/are rejected.

7)☒ Claim(s) *2-4,13-15,18-19,23 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/10/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

1. The abstract of the disclosure is objected to because of the following minor errors:

   a. Line 1 reads, "The present invention provides an apparatus and method for ..." it is suggested that this be changed to "An apparatus and method for...".

   b. It is suggested that all reference characters be removed from the abstract.

Correction is required. See MPEP § 608.01(b).

2. The disclosure is objected to because of the following informalities: Page 4, line 2 reads " ... and the clock pulse **makes only** sense and works only when data symbol..." It is suggested that this be changed to "... and the clock pulse **only makes** sense and works only when data symbol...".

Appropriate correction is required.

Claim Objections

3. Claims 3 and 10 are objected to because of the following informalities:

   a. Claim 3 states that it is dependent upon "claim 1" but examiner believes it should state that it is dependent upon "claim 2".

   b. Claim 10 recites the limitation "comprises an infrared signal, preferably a 4-PPM signal. It is suggested that "preferably a 4-PPM signal" be omitted or the claim be changed to read, "comprises a 4-PPM infrared signal".

   c. Claims 2-4, 13-15, 18-19, 23 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5-8, 10-12, 17, 20-21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagidaira, US Patent No. 3,987,422.

6. Regarding claim 1, Yanagidaira discloses an apparatus for determining the quality of a digital signal, comprising a limiter for sampling the digital signal; an edge detector for detecting an edge of a pulse of the sampled digital signal (see figure 5, block 12); a counter for counting the clock cycles between edges detected by the edge detector (See figure 5, block 13 and column 3, lines 1-5); and a deviation detector being able to compare the counted clock cycles with a pre-stored reference value in order to provide a deviation value as a measure for the instantaneous quality of the digital signal (See column 3, lines 1-5). Yanagidaira fails to disclose a sampler that uses clock cycles for sampling the digital signal. However, Yanagidaira does disclose a hard limiter, which samples the received digital signal. The limiter of Yanagidaira samples the received wave by clipping the wave and reshaping it into a rectangular wave. The function of the limiter in Yanagidaira does not differ from the function of the sampler as claimed in the current application. A sampler using clock cycles is used to take uniform samples within a nominal time span/pulse width. The claim states that the number of samples taken in a nominal pulse width is greater than or EQUAL to 1. The limiter samples the received digital signal once

in the pulse width. Claim limitations are met with Yanagidaira. It would have been obvious to one of ordinary skill in the art to use a sampler with a clock or a limiter to sample a digital signal.

7. Regarding claim 5, which inherits all of the limitations of claim 1, Yanagidaira discloses an apparatus for determining the quality of a digital signal, wherein the edge detector (See figure 5, block 12) bases edge detection on a first sample value and at least one second sample value (See column 3, lines 1-5).

8. Regarding claim 6, which inherits all of the limitations of claim 1, Yanagidaira discloses an apparatus for determining the quality of a digital signal, wherein the counter comprises an up counter, preferably a modulo N counter, where N is an integer number (See column 6, lines 43-54).

9. Regarding claim 7, which inherits all of the limitation of claim 1, Yanagidaira discloses an apparatus for determining the quality of a digital signal, wherein the deviation detector comprises a comparator that provides a positive or negative deviation value (See column 2, lines 19-27).

10. Regarding claim 8, which inherits all of the limitations of claim 1, Yanagidaira discloses an apparatus for determining the quality of a digital signal, wherein the digital signal is encoded by a pulse modulation (See column 1, lines 20-22), preferably a Pulse Position Modulation, and wherein the digital signal represents data carried in frames comprising at least a header field which contains a preamble and a data field (See column 1, lines 22-26).

11. Regarding claim 10, which inherits all of the limitations of claim 1, Yanagidaira discloses an apparatus for determining the quality of a digital signal, wherein the digital signal comprises a pulse modulated signal (See column 1, lines 20-22). Yanagidaira fails to disclose an infrared

signal. However, it is well known in the art that and infrared signals are transmitted using a pulse modulation. It would have been obvious to one skilled in the art to use an infrared signal since it is a pulse modulated signal.

12. Regarding claim 11, which inherits all of the limitations of claim 1, Yanagidaira discloses an apparatus for determining the quality of a digital signal. Yanagidaira fails to disclose an apparatus for determining the quality of a digital signal wherein the digital signal comprises noisy signals containing no data. However, it is well known in the art that when the noise amplitude is much greater than the signal amplitude, when the two signals are combined it will appear as if there is no data. It would have been obvious to one skilled in the art to state that the digital signal is a noisy signal with no data since the data cannot be recognized over the noise.

13. Regarding claim 12, Yanagidaira discloses an apparatus for determining the quality of a digital signal, comprising a limiter for sampling the digital signal; an edge detector for detecting an edge of a pulse of the sampled digital signal (see figure 5, block 12); a counter for counting the clock cycles between edges detected by the edge detector (See figure 5, block 13 and column 3, lines 1-5); and a deviation detector being able to compare the counted clock cycles with a pre-stored reference value in order to provide a deviation value as a measure for the instantaneous quality of the digital signal (See column 3, lines 1-5). Yanagidaira fails to disclose a sampler that uses clock cycles for sampling the digital signal. However, Yanagidaira does disclose a hard limiter, which samples the received digital signal. The limiter of Yanagidaira samples the received wave by clipping the wave and reshaping it into a rectangular wave. The function of the limiter in Yanagidaira does not differ from the function of the sampler as claimed in the

current application. It would have been obvious to one of ordinary skill in the art to use a sampler with a clock or a limiter to sample a digital signal.

14. Regarding claim 17, Yanagidaira discloses a method for determining the quality of a digital signal, the method comprising the steps of: sampling the digital signal width with a number n of samples per defined pulse, whereby $n \geq 1$ (See figure 5, block 11 and rejection to claim 1); detecting an edge of a pulse of the sampled digital signal (See figure 5, block 12); counting the clock cycles between edges (See column 3, lines 1-5); and comparing the counted clock cycles with a pre-stored reference-value in order to output a deviation value as a measure for the instantaneous quality of the digital signal (See column 2, lines 33-36).

15. Regarding claim 20, which inherits all of the limitations of claim 17, Yanagidaira discloses a method for determining the quality of a digital signal further comprising the step of detecting a first digital signal having the best signal quality measure (PCS) and selecting it for further processing (See figure 9, decoder, block 22).

16. Regarding claim 21, which inherits all of the limitations of claim 20, Yanagidaira discloses a method for determining the quality of a digital signal further comprising the step of detecting a second digital signal having the second-best signal quality measure (DCS) and selecting these signal (PCS. DCS) for further processing. (See figure 9, decoder, block 22).

17. Regarding claim 24, which inherits the limitations of claim 17, Yanagidaira discloses a method for determining the quality of a digital signal, wherein the deviation value and/or the signal quality measure are/is determined for at least two digital signals, preferably for three digital signals (See column 2, lines 2-5).

18. Claims 9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagidaira, US Patent No. 3,987,422 in view of Shen, US Patent No. 6,625,231.

19. Regarding claim 9, which inherits all of the limitations of claim 8, Yanagidaira discloses an apparatus for determining the quality of a digital signal. Yanagidaira fails to disclose an apparatus wherein the quality of the digital signal is determinable within the preamble. However, Shen discloses an adaptive phase demodulation apparatus and method where the phase compensation controller is responsive to the phase error and signal strength. Synchronization is accomplished during the preamble portion of the frame. It would have been obvious to one of ordinary skill in the art to determine the quality of the signal for synchronization during the preamble as Shen discloses while using the apparatus of Yanagidaira because then nearly no delays would occur and the best signal or signals could be chosen immediately.

20. Regarding claim 22, which inherits all of the limitations of claim 17, Yanagidaira discloses a method for determining the quality of a digital signal. Yanagidaira fails to disclose a method wherein the quality of the digital signal is determinable within the preamble. However, Shen discloses an adaptive phase demodulation apparatus and method where the phase compensation controller is responsive to the phase error and signal strength. Synchronization is accomplished during the preamble portion of the frame. It would have been obvious to one of ordinary skill in the art to determine the quality of the signal for synchronization during the preamble as Shen discloses while using the method of Yanagidaira because then nearly no delays would occur and the best signal or signals could be chosen immediately.

Allowable Subject Matter

21. Claims 16 and 25 are allowed.

22. The following is a statement of reasons for the indication of allowable subject matter:

a. Regarding claim 16, there is no prior art that teaches a receiver system including a channel multiplexer having logic including a minimum-maximum detector for detecting a first digital signal with best signal quality measure and a second digital signal with second-best quality measure and a diversity multiplexer for selecting these digital signals for further processing and **a channel detector for determining a pulse position that bases on the first digital signal with the best signal quality measure and the second digital signal with the second-best signal quality measure, the apparatus comprising: a first storage unit for storing at least one symbol of the first digital signal with the best signal quality measure; a second storage unit for storing at least one symbol of the second digital signal with the second-best signal quality measure; and a determination unit comprising a probability table, which in case that the first and second digital signals are received is addressed with the at least one symbol of the first digital signal with the best signal quality measure and the at least one symbol of the second digital signal with the second-best signal quality measure, thereby providing a value that is defined as the pulse position**.

b. Regarding claim 25, there is no prior art that teaches a method for determining quality of a digital signal comprising sampling the digital signal with a number n of samples per defined pulse width, whereby $n \geq 1$; detecting an edge of a pulse of the sampled digital signal; counting the clock cycles between edges; and comparing the counted clock cycles with a pre-stored reference value in order to output a deviation value as a measure for the instantaneous quality of the digital signal; and **further comprising the following steps**

for determining a pulse position for the digital signal, which is received as at least a first digital signal and a second digital signal: storing a probability table; storing at least one symbol of the first digital signal; storing at least one symbol of the second digital signal; and addressing the probability table with the at least one symbol of the first digital signal and the at least one symbol of the second digital signal, thereby the probability table providing a value that is defined as the pulse position.

The bolded limitations in combination with the signal quality determination method and apparatus limitations are what make these claims allowable over prior art. There is no art that teaches these limitations in combination.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a. McCabe, US Patent No. 5,297,164 discloses a digital communications system.

b. Kim, US Patent No. 5,719,904 discloses a data restoring circuit.

c. Behrin, US Patent No. 5,761,254 discloses a digital architecture for recovering NRZ/NRZI data.

d. Crittenden, US Patent No. 5,903,605 discloses a jitter detection method and apparatus.

e. Kumaki, US Patent No. 6,549,598 B1 discloses a clock signal extraction circuit.

f. Park et al., US Patent No. 6,580,775 B1 discloses a method for detecting frequency of digital phase locked loop.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Krista M. Flanagan whose telephone number is (571) 272-2203. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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